PCIe EP

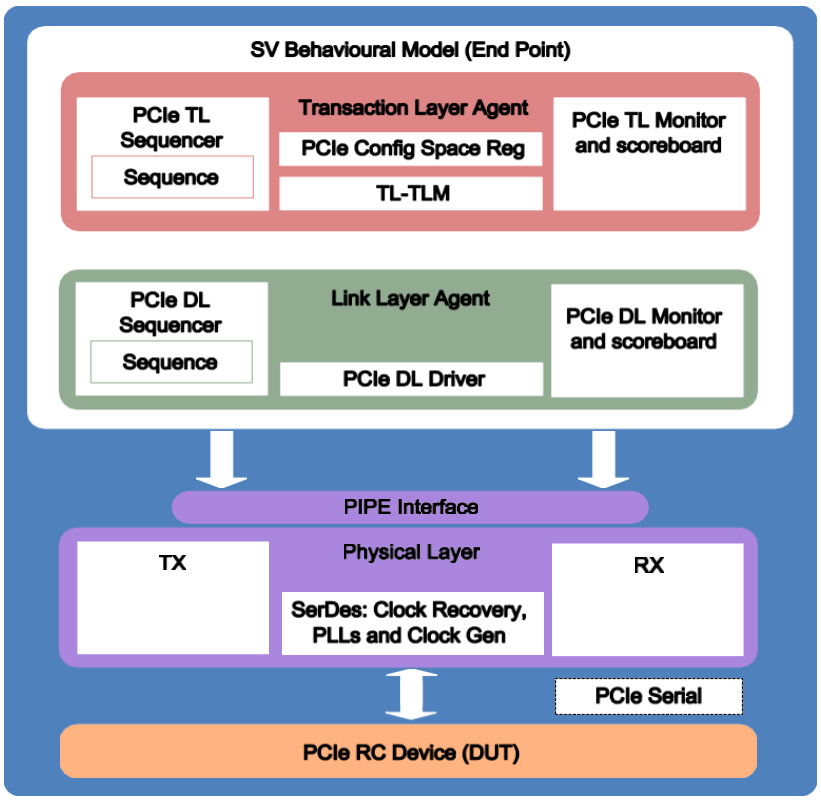
asureVIP

PCIe End Point (EP) UVM VIP

Tessolve Semiconductors offers PCIe End Point (EP) VIP as part of its asureVIP series of offerings. This is a highly flexible and configurable verification IP which can be easily, integrated into any IP Subsystem verification environment, SOC verification environment and Emulation platforms.

The VIP comes with a Bus Monitor for performing all protocol checks. The monitor performs protocol checks and reports errors for non-compliance with PCIe Specification reference.

Block Diagram



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TESSOLVE
A Hero Electronix Venture

Overview

VIP: PCIe EP

Compliance: PCI Express Base 2.1 Spec

Language: System Verilog, C or C++

Methodology: UVM 1.1

Simulators: Cadence Incisive, Mentor Questa, Aldec Riviera-PRO

Deliverables

- PCIe EP VIP
- Interface to software above transaction layer
- Traffic generator functions for SoC level verification
- Sample Testbench integrated with VIP
- Sample Virtual Sequencer
- VIP User Guide

Key Benefits

- Highly Flexible, Independent and Configurable PCIE VIP in EP mode
- Some layers of the VIP are synthesizable
- Can be used on Emulation platforms

Technical Specifications

- Independently controlled egress, ingress traffic, and support for all types of packets
- PCIe and legacy interrupt support
- Gen1 and Gen2 support with optional top speed as Gen1
- Support for Multiple VCs and Multiple TCs
- RAL model for all configuration space registers with back door access
- Flow Control checks and ordering rule monitors
- Full set DLLP Support
- DL Control and Management state machine with FC initialization
- Configurable ACK frequency, FC update frequency and update timer
- Independent LTSSM Monitor
- Auto speed negotiations
- ASPM and PCIEPM support
- Complete Ordered Set support
- Compliance and Loopback mode support

Other VIPs Available

- **ARM**: AXI, APB, AMBA ACE and CHI
- **Hi-Speed Interface**: Ethernet (10/100/1000MB & 10GB), PCIe RC and EP, USB 3.0 Host and Device, CSIX and SPI
- **Memory and Storage**: SDCARD 4.0, DDR 4/3, LPDDR 4/3 and ONFI
- **MIPI**: DPHY, DSI, LPDDR, MPHY, SMBUS, RFFE and Unipro
- **Universal Serial I/O**: CAN, GPIO, I2C, UART, SPDIF, I2S, SMBUS, SPI and TDM

Independent Verification Service

Tessolve can deliver an independent verification service that not only reduces development costs and time-to-to-market, but also improves product quality.

Proven Implementations

Use asureVIP with the confidence of knowing that they have been successfully deployed by leading SoC companies around the world.

About Tessolve

Tessolve Semiconductors Private Limited provides services and products to organizations developing complex products in the microelectronics and embedded software and systems industries.

Tessolve operates globally with offices in the UK, France, Germany, India, Singapore the USA plus a network of international partners.

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